CompactFlash Card

AC60-XXXXR04XX

Table of Contents

Revision History

Revision	Date	History	Remark
A.0	11/29 '05	New Creation	
A.1	01/12 '06	Feature Modify	
A.2	01/20 '06	Electrical Specification Modify	
A.3	02/09 '06	Feature Modify	
A.4	03/24 '06	Feature & Electrical Specification Modify	
A.5	04/10 '06	Feature & Electrical Specification Modify	
A.6	06/30 '06	Modify the Format	
A.7	07/18 '06	Add the Features	

1. Description

AC60-XXXX is **CompactFlash™** based on flash memory controller technology. This card complies with **CompactFlash™** specification, it is suitable for the usage of data storage memory for PC or other electric equipment and digital still camera. This card is equipped with NAND flash memory. By using this card it is possible to operate stability for the system that have **CompactFlash™** slots.

Fixed mode (045A)~AC60-XXXX-XXX2(4) disk use in system storage, some operating system can not accept boot-up from removable mode (848A)~AC60-XXXX-XXX1(3) disk like windows XP, when we boot-up from CFC with windows XP, the system detect the device will disable Removable device boot-up function, so the system can not finish the boot-up process. For this issue, we can setting the device mode to Fixed mode (045A) to solve this problem.

The CFC setting to Fixed or Removable mode will no any function different or issue.

2. Features

- 32Mbytes~8Gbytes flash memory card.
- CompactFlash™ specification: PCMCIA ver.2.1 and PC Card ATA ver.2.01 compatible 50pin SMT connector and type I (3.3mm).
- 3.3V/5V single power supply operation.
- Internal self-diagnostic program operates at VCC power on.
- 3 variations of access mode:
  - Memory Card Mode.
  - I/O Card Mode.
  - True-IDE Mode.
- High reliability based on internal ECC (Error Correcting Code) Function.
- Data reliability is 1 error in 10^{14} bits read.
- Support PIO Mode4 and Ultra DMA mode2.
- Temperature range : 0 to 70 ℃.(Industrial type)
  -40 to 85 ℃.(wide type)
- Power Consumption (3.3V/ 5.0V).
  - Active mode: 29.4mA/ 34.4mA (3.3v/ 5.0v).
  - Sleep mode: 7.3 mA / 7.7mA (3.3v/ 5.0v).
- Write protect for read only function (only for AC60-XXXX-XXX1(2,3,4))
- High Performance:
  - Read: Up to 16.4Mbytes/s
  - Write: Up to 14.32Mbytes/s

Notes: The performance will depends on different platform with different test result.

3. Interface Description

3.1 Card pin Assignment

	Memory card mode		I/O card mode		True IDE mode	
Pin NO.	**Signal name**	**I/O**	**Signal name**	**I/O**	**Signal name**	**I/O**
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CE1	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATASEL	I
10	A9	I	A9	I	A9	I
11	A8	I	A8	I	A8	I
12	A7	I	A7	I	A7	I
13	VCC	—	VCC	—	VCC	—
14	A6	I	A6	I	A6	I
15	A5	I	A5	I	A5	I
16	A4	I	A4	I	A4	I
17	A3	I	A3	I	A3	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOIS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	-CE2	I	-CE2	I	-CE2	I
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD	I
35	-IOWR	I	-IOWR	I	-IOWR	I
36	-WE	I	-WE	I	-WE	I
37	RDY/-BSY	O	-IREQ	O	INTRQ	O
38	VCC	—	VCC	—	VCC	—
39	-CSEL	I	-CSEL	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	-RESET	I
42	-WAIT	O	-WAIT	O	IORDY	O
43	-INPACK	O	-INPACK	O	-INPACK	O
44	-REG	I	-REG	I	-REG	I
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	—	GND	—	GND	—

3.2 Card pin Description

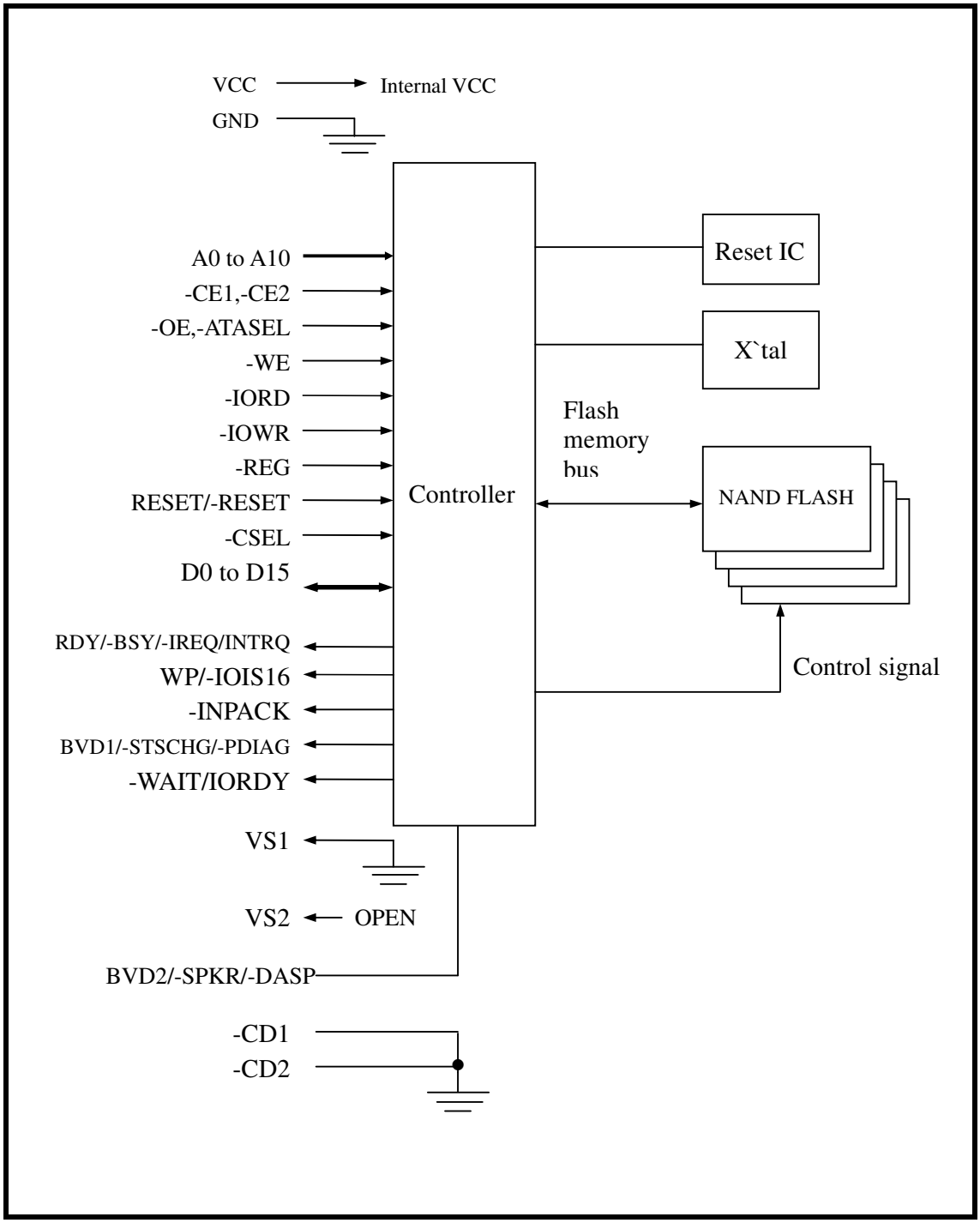
Signal Name	Dir	Pin No.	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12,14,15,16,17,18,19,20	These address lines along with the-REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF + Card, the memory mapped port add address registers within the CompactFlash Storage Card or CF+ Card , a byte in the card's information structure and its configuration control and status registers.
A10 to A0 (PC Card I/O Mode)			
A2 to A0 (True IDE Mode)		18,19,20	In True IDE Mode only A {2:0} are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as BVD1 is not supported
-STSCHG (PC Card Memory Mode)			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states; while the I/O interface is configured. Its use is controlled by the Card Configured and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card / I/O Mode)			This line is the Binary AUDIO OUTPUT FROM THE CARD .if the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave
-CD1,-CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompcatFlash Storage Card or CF + Card. They are used by the host to determine that the CompactFlash Storage Card or CF +Card is fully inserted into its socket.
-CE1,-CE2 (PC Card I/O Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A1.-CE1,-CE2 allows 8 bit hosts to access all data on D0 to D7. See Access specification below.
-CE1,-CE2 (PC Card I/O Mode)			
-CS0,-CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pins is open, this device is configured as a Slave.
-CSEL (True IDE Mode)			

Signal Name	Dir	Pin No.	Description
D15 to D00 (PC Card Memory Mode)	I/O	31,30,29,28,27,49,48,47,6,5,4,3,223,22,21	These lines carry the Data, Commands and Status information between the host and the controller.D00 is the LSB of the Even Byte of the Word.D08 is the LSB of the Even Byte of the Word.D08 is the LSB of the Odd Byte of the Word.
D15 to D00 (PC Card I/O Mode)			
D15 to D00 (True IDE Mode)			True IDE Mode, all Task File operations occur in byte mode on the low order bus D00 to D07 while all data transfers are 16 bit using D00 to D15.
GND (PC Card Memory Mode)	—	1,50	Ground
GND (PC Card I/O Mode)			
GND (True IDE Mode)			
-INPCAK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF +Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF +Card and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF +Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompcatFlash Storage Card or CF +Card controller registers when the CompactFlash Storage Card or CF +Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (Trailing edge)
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Signal Name	Dir	Pin No.	Description
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF +Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode. This signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash Storage Card or CF +Card is ready to accept a new data transfer operation and held low when the card is busy . The Host memory card socket must provide a pull-up resistor. At power up and at Reset the RDY/-BSY signal is held low (busy) until the CompactFlash Storage Card or CF +Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF +Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true. The CompactFlash Storage Card or CF +Card has been powered up with + RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			Operation-After the CompactFlash Storage Card or CF + Card has been configured for I/O operation; this signal is used as interrupt Request. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high interrupt Request to the host.
-REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register(Attribute) Memory accesses. High for Common Memory. Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
RESET (PC Card Memory Mode)	I	41	When the pin is high, this signal Resets the CompactFlash Storage Card or CF +Card. The CompcatFlash Storage Card or CF +Card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF +Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset form the host.

Signal Name	Dir	Pin No.	Description
VCC (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	–	13,38	+5V +3.3V power.
-VS1 /-VS2 (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O	33,40	Voltage Sense Signals. –VS1 is grounded so that the CompactFlash Storage Card or CF + Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
-WAIT (PC Card Memory Mode)	O	42	The –WAIT signal is driven low by the CompactFlash Storage Card or CF +Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
IORDY (True IDE Mode)			In True IDE Mode this output signal may be used as IORDY
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for starting memory write data to the registers of the CompactFlash Storage Card or CF + Card when the card is configured I the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	Memory Mode-The CompactFlash Storage Card or CF + Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation-When the CompactFlash Storage Card or CF + Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16)function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.3 Card Block Diagram



4. Access specification

4.1 Attribute access specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of –REG = "L" as follows. That region can be accessed by Byte/Word/Odd-byte modes, which are defined by PC card standard specifications.

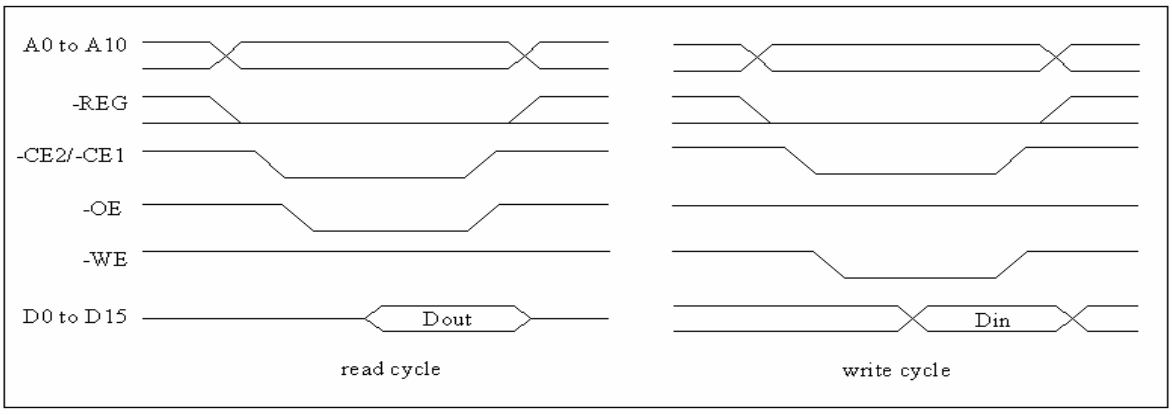
Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	High-Z	High-Z
Byte access (8-it)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	invalid
Word access (16-it)	L	L	L	X	L	H	invalid	even byte
Odd byte access (8bit)	L	L	H	X	L	H	invalid	High-Z
Note: X → L or H								

Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	Don't care	Don't care
Byte access (8bit)	L	H	L	L	H	L	Don't care	even byte
	L	H	L	H	H	L	Don't care	Don't care
Word access (16bit)	L	L	L	×	H	L	Don't care	even byte
Odd byte access (8bit)	L	L	H	×	H	L	Don't care	Don't care
Note: X → L or H								

Attribute Access Timing Example



4.2 Task file Register access specifications

There are two cases of Task File register mapping, one is mapped I/O address area, the other is mapped Memory address area. Each case of Task File registers read and write operations is executed under the condition as follows. That area can be accessed by Byte/World/Odd Byte modes, which are defined by PC card standard specifications.

4.2.1 I/O address map

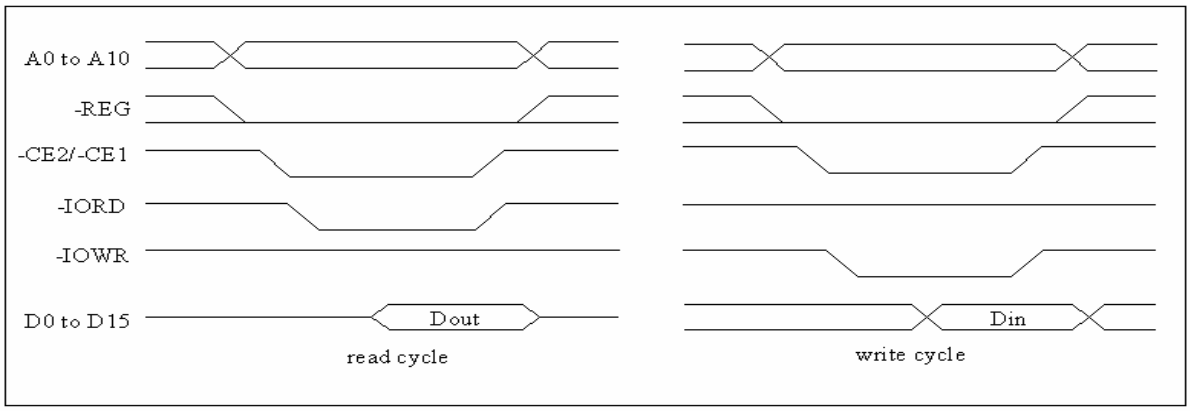
Task File Register Read Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	High-Z	High-Z
Byte access (8bit)	L	H	L	L	L	H	H	H	High-Z	even byte
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16bit)	L	L	L	X	L	H	H	H	odd byte	even byte
Odd byte access (8bit)	L	L	H	X	L	H	H	H	odd byte	High-Z
Note: X→ L or H										

Task File Register Write Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	Don't care	Don't care
Byte access(8-bit)	L	H	L	L	H	L	H	H	Don't care	even byte
	L	H	L	H	H	L	H	H	Don't care	odd byte
Word access(16-bit)	L	L	L	×	H	L	H	H	odd byte	even byte
Odd byte access(8-bit)	L	L	H	×	H	L	H	H	odd byte	don't care
Note: X→ L or H										

Task File Register Access Timing Example (1)



4.2.2 Memory address map

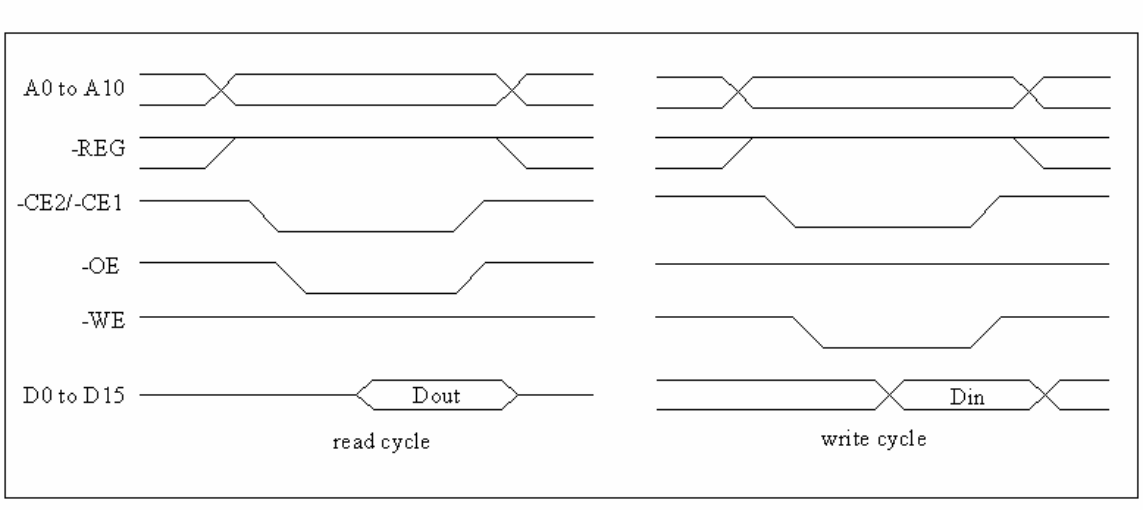
Task File Register Read Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	High-Z	High-Z
Byte access (8bit)	H	H	L	L	L	H	H	H	High-Z	even byte
	H	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16bit)	H	L	L	X	L	H	H	H	odd byte	even byte
Odd byte access (8bit)	H	L	H	X	L	H	H	H	odd byte	High-Z
Note: X→ L or H										

Task File Register Write Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	Don't care	Don't care
Byte access (8bit)	H	H	L	L	H	L	H	H	Don't care	even byte
	H	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16bit)	H	L	L	X	H	L	H	H	odd byte	even byte
Odd byte access (8bit)	H	L	H	X	H	L	H	H	odd byte	don't care
Note: X→ L or H										

Task File Register Access Timing Example (2)



4.2.3 True IDE Mode

The card can be configured in a True IDE This card is configured in this mode only when the –OE input signal is asserted GND by the host. In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operation to the task file and data register is allowed. If this card is configured during power on sequence, data register is accessed in word (16-bit). The card permits 8-bit accessed if the user issues a Set Feature Command to put the device in 8-bit mode.

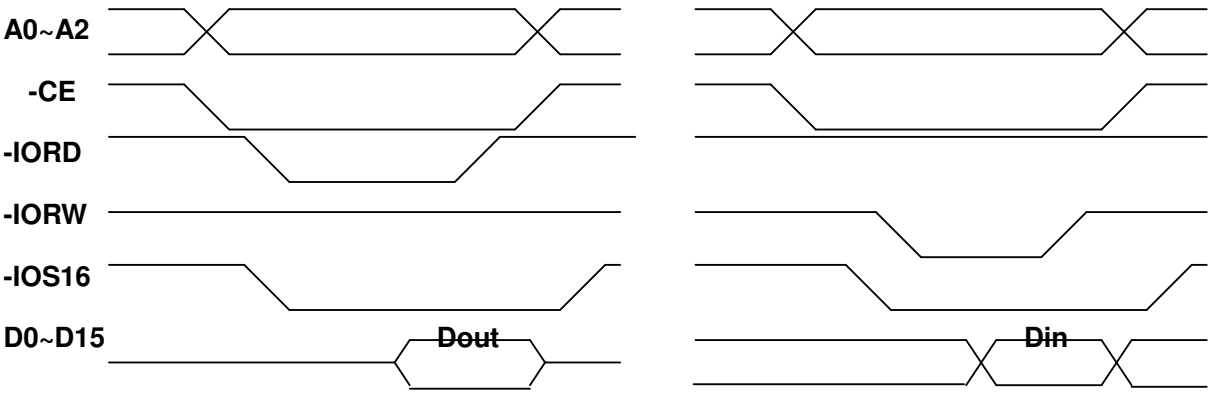
True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0~A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode	L	L	X	X	X	High-Z	High-Z
Standby mode	H	H	X	X	X	High-Z	High-Z
Data register access	H	L	0	L	H	Odd byte	even byte
Alternate status access	L	H	6H	L	H	High-Z	Status out
Other task file access	H	L	1~7H	L	H	High-Z	Data
Note: X→ L or H							

True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0~A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode	L	L	X	X	X	Don't card	Don't card
Standby mode	H	H	X	X	X	Don't card	even byte
Data register access	H	L	0	H	L	Odd byte	Don't card
Alternate status access	L	H	6H	H	L	Don't card	Control in
Other task file access	H	L	1~7H	H	L	Odd byte	Data
Note: X→ L or H							

True IDE Mode I/O Access Timing Example



4.3 Configuration register specification

This card supports four Configuration registers for the purpose of the configuration and observation of this card.

4.3.1. Configuration Option register (Address 200H)

This register is used for the configuration of the card configuration status and for the issuing soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevIREQ	INDEX					
Note: initial value: 00H							

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to “1”, places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to “0”,places the card in the reset state of Hard Reset (This bit is set to “0” by Hard Reset). Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.
LevIREQ (HOST->)	R/W	This bit sets to “0” when pulse mode interrupt is selected, and “1” when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bits is used for select operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is “000000” for the purpose of Memory card interface recognition.
Note: initial value → 00H		

INDEX bit assignment

INDEX bit								
5	4	3	2	1	0	Card mode	Task File register address	Mapping mode
0	0	0	0	0	0	Memory card	0H to FH, 400H to 7FFH	memory mapped
0	0	0	0	0	1	I/O card	××0H to ××FH	Contiguous I/O mapped
0	0	0	0	1	0	I/O card	1F0H to 1F7H, 3F6H to 3F7H	Primary I/O mapped
0	0	0	0	1	1	I/O card	170H to 177H, 376H to 377H	Secondary I/O mapped

4.3.2. Configuration and Status register (Address 202H)

This register is used for observing the card state.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0
Note: initial value: 00H							

Name	R/W	Function
CHGED (CARD->)	R	This bit indicates that CRDY-BSY bit on Pin Replacement register is set to “1”. When CHGED bit is set to “1”, -STSCHG pin is held “L” at the confition of SIGCHG bit set to “1” and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set to “1”, -STSCHG pin is controlled by CHGED bit. If this bit is set to “0”, -STSCHG pin is kept “H”.
IOIS8 (HOST->)	R/W	The host sets this field to “1” when it can provide I/O cycles only with on 8bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to “1”, the card enters sleep state (Power Down mode). When this bit is reset to “0”, the card transfers to idle state (active mode). RRDY/-BSY bit on Pin Replacement Register becomes BUSY when this bit is changed. RRDY/-BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle, and powers back up when it receives a command.
INTR (CARD->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition which cased the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is a zero.

4.3.3. Pin Replacement register (Address 204H)

This register is used for providing the signal state of –IREQ signal when the card configured I/O card interface.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CRDY/-BSY	0	1	1	RRDY/-BSY	0
Note: initial value: 00H							

Name	R/W	Function
CRDY/-BSY (HOST->)	R/W	This bit is set to “1” when the RRDY/-BSY bit changes state. This bit may also be written by the host.
RRDY/-BSY (HOST->)	R/W	When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/-Bsy bit masking.

4.3.4. Socket and Copy register (Address 206H)

This register is used for identification of the card from the other card. Host can read and write this register. This register should be set by host before this card’s Configuration Option register set.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	0	0	0	0
Note: initial value: 00H							

Name	R/W	Function
DRV# (HOST->)	R/W	This fields are used for the configuration of the plural cards. When host configures the plural cards, written the card’s copy number in this field. In this way, host can perform the card’s master/slave organization.

4.4 CIS Information

CIS information of Compact Flash Card are defined as follows.

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
000H	01H	CISTPL_DEVICE								Device Info tuple	Tuple code
002H	03H	TPL_LINK								Link length is 3 byte	Link to next tuple
004H	D9H	Device Type				W	Speed			Type=D: I/O device WPS=1: no WP switch Speed=1: 250 ns	Device type, WPS, speed
006H	01H	# address units –1					unit size			2 Kbytes of address space	Device size
008H	FFH	CISTPL_END								End of CISTPL_DEVICE	End marker
00AH	1Ch	CISTPL_DEVICE_OC								Common memory other operating conditions tuple	Tuple code
00CH	04H	TPL_LINK								Link length is 4 byte	Link to next tuple
00EH	02H	Ext	Reserved					3V	M	3V=1: dual voltage card, conditions for 3.3V operation M=0: conditions without wait	Other Conditions Information
010H	D9H	Device Type				W	Speed			Type=D: I/O device WPS=1: no WP switch Speed=1: 250 ns	Device type, WPS, speed
012H	01H	# address units –1					unit size			2 Kbytes of address space	Device size
014H	FFH	CISTPL_END								End of CISTPL_DEVICE_OC	End marker
016H	18H	CISTPL_JEDEC_C								JEDEC programming info tuple	Tuple code
018H	02H	TPL_LINK								Link length is 2 byte	Link to next tuple
01AH	DFH	JEDEC ID								Device manufacturer ID	Manufacturer ID
01CH	01H	JEDEC Info								Manufacturer specific info	Manufacturer info
01EH	20H	CISTPL_MANFID								Manufacturer ID tuple	Tuple code
020H	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
022H	00H	TPLMID_MANF								PC Card manufacturer code	Manufacturer ID
024H	00H										
026H	00H	TPLMID_CARD								Manufacturer specific info	Manufacturer info
028H	00H										
02AH	21H	CISTPL_FUNCID								Function ID tuple	Tuple code
02CH	02H	CISTPL_LINK								Link length is 2 bytes	Link to next tuple
02EH	04H	TPLFID_FUNCTION								Fixed disk drive	Function code
030H	01H	Reserved						R	P	R=0: no expansion ROM P=1: configure at POST	System init byte TPLFID_SYSINIT
032H	22H	CISTPL_FUNCE								Function Extension tuple	Tuple code
034H	02H	CISTPL_LINK								Link length is 2 bytes	Link to next tuple
036H	01H	Disk function extension tuple								Disk interface information	TPLFE_TYPE
038H	01H	Disk interface type								PC card ATA interface	TPLFE_DATA
03AH	22H	CISTPL_FUNCE								Function Extension tuple	Tuple code
03CH	03H	CISTPL_LINK								Link length is 3 bytes	Link to next tuple

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
03EH	02H	Disk function extension tuple								PC card ATA basic features	TPLFE_TYPE
040H	04H	Reserved			D	U	S	V		D=0: single drive on card U=0: no unique serial number S=1: silicon device V=0: no V_{PP} required	TPLFE_TYPE
042H	07H	R	I	E	N	P				I=0: twin IOIS16# unspecified E=0: index bit not emulated N=0: I/O includes 0x3F7 P=7: sleep, standby, idle supported	TPLFE_TYPE
044H	1AH	CISTPL_CONFIG								Configuration Tuple	Tuple code
046H	05H	TPL_LINK								Link length is 5 bytes	Link to next tuple
048H	01H	RFS		RMS				RAS		RFS: reserved RMS: 1 byte register mask RAS: 2 bytes base address	Size of fields TPCC_SZ
04AH	07H	TPCC_LAST								Last configuration entry is 07H	Last entry index
04CH	00H	TPCC_RADR (LSB)								Configuration registers are located at 0200H	Configuration register location
04EH	02H	TPCC_RADR (MSB)									
050H	0FH	TPCC_RMSK								Configuration registers 0 to 3 are present	Configuration reg-ister present mask
052H	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
054H	0BH	CISTPL_LINK								Link length is 11 bytes	Link to next tuple
056H	C0H	I	D	Configuration Index						Memory mapped configuration, index=0 I=1: Interface byte follows D=1: Default entry	Configuration Table Index Byte TPCE_INDX
058H	C0H	W	R	P	B	Interface type				W=1: wait required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=0: Memory interface	Interface Description TPCE_IF
05AH	A1H	M	MS		IR	IO	T	Power		M=1: misc info present MS=1: 2 byte memory length IR=0: no interrupt is used IO=0: no I/O space is used T=0: no timing info specified Power=1: V_{CC} info, no V_{PP}	Feature Selection Byte TPCE_FS
05CH	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	Power Description Structure Parameter Selection Byte TPCE_PD
05EH	55H	X	Mantissa				Exponent			Nominal voltage 5.0V	
060H	4DH	X	Mantissa				Exponent			Minimum voltage 4.5V	
062H	5DH	X	Mantissa				Exponent			Maximum voltage 5.5V	
064H	75H	X	Mantissa				Exponent			Peak current 80 mA	

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
066H	08H	Length in 256 byte units (LSB)								Length of memory space is 2 Kbytes	Memory space-descr. TPCE_MS
068H	00H	Length in 256 byte units (MSB)									
06AH	21H	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	Miscellaneous features TPCE_MI
06CH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
06EH	06H	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
070H	00H	I	D	Configuration Index						Memory mapped configuration, index=0	TPCE_INDX
072H	01H	M	MS		IR	IO	T	Power		Power=1: V_{CC} info, no V_{PP}	TPCE_FS
074H	21H	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
076H	B5H	X	Mantissa				Exponent			X=1: extension byte present	
078H	1EH	X	Extension							Nominal voltage 3.30V	
07AH	4DH	X	Mantissa				Exponent			Peak current 45 mA	
07CH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
07EH	0DH	CISTPL_LINK								Link length is 13 bytes	Link to next tuple
080H	C1H	I	D	Configuration Index						I/O mapped, index=1 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
082H	41H	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
084H	99H	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: V_{CC} info, no V_{PP}	TPCE_FS
086H	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
088H	55H	X	Mantissa				Exponent			Nominal voltage 5.0V	
08AH	4DH	X	Mantissa				Exponent			Minimum voltage 4.5V	
08CH	5DH	X	Mantissa				Exponent			Maximum voltage 5.5V	
08EH	75H	X	Mantissa				Exponent			Peak current 80 mA	
090H	64H	R	S	E	IO					S=1: support 16 bit hosts E=1: support 8 bit hosts IO=4: 4 address lines decoded	TPCE_IO

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
092H	F0H	S	P	L	M	V	B	I	N	S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=1: masks V..N present V=0: no vendor unique IRQ B=0: no bus error IRQ I=0: no I/O check IRQ N=0: no NMI	TPCE_IR
094H	FFH	IRQ7..0								Interrupt signal may be assigned to any host IRQ	
096H	FFH	IRQ15..8									
098H	21H	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
09AH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
09CH	06H	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
09EH	01H	I	D	Configuration Index						I/O mapped, index=1	TPCE_INDX
0A0H	01H	M	MS		IR	IO	T	Power		Power=1: V_{CC} info, no V_{PP}	TPCE_FS
0A2H	21H	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
0A4H	B5H	X	Mantissa				Exponent			X=1: extension byte present	
0A6H	1EH	X	Extension							Nominal voltage 3.30V	
0A8H	4DH	X	Mantissa				Exponent			Peak current 45 mA	
0AAH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0ACH	12H	CISTPL_LINK								Link length is 18 bytes	Link to next tuple
0AEH	C2H	I	D	Configuration Index						I/O mapped, index=2 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
0B0H	41H	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
0B2H	99H	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: V_{CC} info, no V_{PP}	TPCE_FS
0B4H	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
0B6H	55H	X	Mantissa				Exponent			Nominal voltage 5.0V	
0B8H	4DH	X	Mantissa				Exponent			Minimum voltage 4.5V	
0BAH	5DH	X	Mantissa				Exponent			Maximum voltage 5.5V	

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
0BCH	75H	X	Mantissa				Exponent			Peak current 80 mA	
0BEH	EAH	R	S	E	IO					R=1: range follows S=1: support 16 bit hosts E=1: support 8 bit hosts IO=10: 10 lines decoded	TPCE_IO
0C0H	61H	LS		AS		NR				LS=1: 1 byte length AS=2: 2 byte address NR=1: 2 address ranges	
0C2H	F0H	Base address 1 (LSB)								Address range 1 0x1F0 to 0x1F7	
0C4H	01H	Base address 1 (MSB)									
0C6H	07H	Address range 1 length									
0C8H	F6H	Base address 2 (LSB)								Address range 2 0x3F6 to 0x3F7	
0CAH	03H	Base address 2 (MSB)									
0CCH	01H	Address range 2 length									
0CEH	EEH	S	P	L	M	IRQN				S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=0: masks V..N not present IRQN=14: use interrupt 14	TPCE_IR
0D0H	21H	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
0D2H	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0D4H	06H	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
0D6H	02H	I	D	Configuration Index						I/O mapped, index=2	TPCE_INDX
0D8H	01H	M	MS		IR	IO	T	Power		Power=1: V_{CC} info, no V_{PP}	TPCE_FS
0DAH	21H	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
0DCH	B5H	X	Mantissa				Exponent			X=1: extension byte present	
0DEH	1EH	X	Extension							Nominal voltage 3.30V	
0E0H	4DH	X	Mantissa				Exponent			Peak current 45 mA	
0E2H	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0E4H	12H	CISTPL_LINK								Link length is 18 bytes	Link to next tuple
0E6H	C3H	I	D	Configuration Index						I/O mapped, index=3 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
0E8H	41H	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
0EAH	99H	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: V_{CC} info, no V_{PP}	TPCE_FS

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
0ECH	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
0EEH	55H	X	Mantissa				Exponent			Nominal voltage 5.0V	
0F0H	4DH	X	Mantissa				Exponent			Minimum voltage 4.5V	
0F2H	5DH	X	Mantissa				Exponent			Maximum voltage 5.5V	
0F4H	75H	X	Mantissa				Exponent			Peak current 80 mA	
0F6H	EAH	R	S	E	IO					R=1: range follows S=1: support 16 bit hosts E=1: support 8 bit hosts IO=10: 10 lines decoded	TPCE_IO
0F8H	61H	LS		AS	NR					LS=1: 1 byte length AS=2: 2 byte address NR=1: 2 address ranges	
0FAH	70H	Base address 1 (LSB)								Address range 1 0x170 to 0x177	
0FCH	01H	Base address 1 (MSB)									
0FEH	07H	Address range 1 length									
100H	76H	Base address 2 (LSB)								Address range 2 0x376 to 0x377	
102H	03H	Base address 2 (MSB)									
104H	01H	Address range 2 length									
106H	EEH	S	P	L	M	IRQN				S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=0: masks V..N not present IRQN=14: use interrupt 14	TPCE_IR
108H	21H	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
10AH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
10CH	06H	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
10EH	03H	I	D	Configuration Index						I/O mapped, index=3	TPCE_INDX
110H	01H	M	MS		IR	IO	T	Power		Power=1: V_{CC} info, no V_{PP}	TPCE_FS
112H	21H	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
114H	B5H	X	Mantissa				Exponent			X=1: extension byte present	
116H	1EH	X	Extension							Nominal voltage 3.30V	
118H	4DH	X	Mantissa				Exponent			Peak current 45 mA	
11AH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
11CH	04H	CISTPL_LINK								Link length is 4 bytes	Link to next tuple
11EH	07H	I	D	Configuration Index						I/O mapped, index=7	TPCE_INDX
120H	00H	M	MS		IR	IO	T	Power		No feature descriptions follow	TPCE_FS

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
122H	28H									Hyperstone specific data	
124H	D3H									Hyperstone specific data	
126H	14H	CISTPL_NO_LINK								No link control tuple	Tuple code
128H	00H	CISTPL_LINK								Link length is 0 bytes	Link to next tuple
12AH	15H	CISTPL_VERS_1								Level 1 version/product info	Tuple code
12CH	0AH	CISTPL_LINK								Link length is 21 bytes	Link to next tuple
12EH	04H	TPPLV1_MAJOR								PCMCIA2.0/JEIDA4.1	Major version
130H	01H	TPPLV1_MINOR								PCMCIA2.0/JEIDA4.1	Minor version
132H	35H									5	Info string “5”
134H	31H									1	Info string “1”
136H	32H									2	Info string “2”
138H	4DH									M	Info string “M”
13AH	42H									B	Info string “B”
13CH	00H									Null terminator	
13EH	20H										Info string “ “
140H	00H									Null terminator	
142H	FFH										
144H	FFH										
146H	FFH										
148H	FFH										
14AH	FFH										
14CH	FFH										
14EH	FFH										
150H	FFH										
152H	FFH										
154H	FFH										
156H	FFH	CISTPL_END								End of CISTPL_VERS_1	End marker
158H	FFH	CISTPL_END								End of CIS	Tuple code

4.5 Task file register specification

There registers are used for reading and writing the storage data in this card. These registers are mapped five types by the configuration of INDEX in Configuration Option register. The decoded addressed are shown as follows.

Memory map (INDEX=0)

-REG	A10	A9~A4	A3	A2	A1	A0	Offset	-OE=L	-WE=L
1	0	X	0	0	0	0	0H	Data register	Data register
1	0	X	0	0	0	1	1H	Error register	Feature register
1	0	X	0	0	1	0	2H	Select count register	Sector count register
1	0	X	0	0	1	1	3H	Sector number register	Sector number register
1	0	X	0	1	0	0	4H	Cylinder lox register	Cylinder low register
1	0	X	0	1	0	1	5H	Cylinder high register	Cylinder high register
1	0	X	0	1	1	0	6H	Drive head register	Drive head register
1	0	X	0	1	1	1	7H	Status register	Command register
1	0	X	1	0	0	0	8H	Dup. Even data register	Dup. Even data register
1	0	X	1	0	0	1	9H	Dup. Odd data register	Dup. Odd data register
1	0	X	1	1	0	1	DH	Dup. Error register	Dup. Feature register
1	0	X	1	1	1	0	EH	Alt. Status register	Dup. Feature register
1	0	X	1	1	1	1	FH	Drive address register	Reserved
1	0	X	X	X	X	0	8H	Even data register	Even data register
1	0	X	X	X	X	1	9H	Odd data register	Odd data register

Contiguous I/O map (INDEX=1)

-REG	A10~A4	A3	A2	A1	A0	Offset	-OE=L	-WE=L
0	X	0	0	0	0	0H	Data register	Data register
0	X	0	0	0	1	1H	Error register	Feature register
0	X	0	0	1	0	2H	Select count register	Sector count register
0	X	0	0	1	1	3H	Sector number register	Sector number register
0	X	0	1	0	0	4H	Cylinder lox register	Cylinder low register
0	X	0	1	0	1	5H	Cylinder high register	Cylinder high register
0	X	0	1	1	0	6H	Drive head register	Drive head register
0	X	0	1	1	1	7H	Status register	Command register
0	X	1	0	0	0	8H	Dup. Even data register	Dup. Even data register
0	X	1	0	0	1	9H	Dup. Odd data register	Dup. Odd data register
0	X	1	1	0	1	DH	Dup. Error register	Dup. Feature register
0	X	1	1	1	0	EH	Alt. Status register	Dup. Feature register
0	X	1	1	1	1	FH	Drive address register	Reserved

Primary map (INDEX=2)

-REG	A10	A9~A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0	X	1FH	0	0	0	0	Data register	Data register
0	X	1FH	0	0	0	1	Error register	Feature register
0	X	1FH	0	0	1	0	Select count register	Sector count register
0	X	1FH	0	0	1	1	Sector number register	Sector number register
0	X	1FH	0	1	0	0	Cylinder lox register	Cylinder low register
0	X	1FH	0	1	0	1	Cylinder high register	Cylinder high register
0	X	1FH	0	1	1	0	Drive head register	Drive head register
0	X	1FH	0	1	1	1	Status register	Command register
0	X	1FH	0	1	1	0	Alt. Status register	Device control register
0	X	1FH	0	1	1	1	Drive address register	Reserved

Secondary I/O map (INDEX=3)

-REG	A10	A9~A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0	X	17H	0	0	0	0	Data register	Data register
0	X	17H	0	0	0	1	Error register	Feature register
0	X	17H	0	0	1	0	Select count register	Sector count register
0	X	17H	0	0	1	1	Sector number register	Sector number register
0	X	17H	0	1	0	0	Cylinder lox register	Cylinder low register
0	X	17H	0	1	0	1	Cylinder high register	Cylinder high register
0	X	17H	0	1	1	0	Drive head register	Drive head register
0	X	17H	0	1	1	1	Status register	Command register
0	X	37H	0	1	1	0	Alt. Status register	Device control register
0	X	37H	0	1	1	1	Drive address register	Reserved

True IDE Mode I/O map

-CE2	-CE1	A3	A1	A0	-INRD=L	-IOWR=L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Select count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder lox register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. Status register	Device control register
0	1	1	1	1	Drive address register	Reserved

1. Data register

This register is a 16-bit register that has read/write ability. And it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register**.**

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

2. Error register

This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to “0”(Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

bit	Name	Function
7	BBK(Bad Block detected)	This bit set when a Bad is detected in requester ID field.
6	UNC(Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF(ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (AboRTed command)	This bit is set if the command has been aborted because of the card status condition.(Not ready. Write fault, Invalid command, etc.)
0	AMNF (Address Mark Not Found	This bit is set in case of a general error.

3. Feature register

This register is write-only register, and provides information regarding features of the drive that the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

4. Sector count register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. IF the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

5. Sector number register

This register contains the starting sector number, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte							

6. Cylinder low register

This register contains the low 8-bit of the starting cylinder address, which is started by following sectors transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte							

7. Cylinder high register

This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte							

8. Drive head register

This register is used for selecting the Drive number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Obsolete	LBA	Obsolete	DRV	Head number			

bit	Name	Function
7	Obsolete	This bit is normally set to “1”
6	LBA	LBA IS A FLAG TO SELECT EITHER Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA =0. CHS mode is selected. When LBA=1.LBA mode is selected. In LBA MODE. The logical Block Address is interrupted as follows: LBA07~LBA00: Sector Number Register D7 to D0. LBA15~LBA08: Cylinder Low Register D7 to D0. LBA23~LBA16: Cylinder High Register D7 to D0. LBA27~LBA24: Drive / Head Register bits HS3 to HS0.
5	Obsolete	This bit is normally set to “1”.
4	DRV (Drive select)	This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

9. Status register

This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX=1,2,3) and level interrupt mode, -IREQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is execting. When this bit is set to “1”, other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to “1”, the card is capable of receiving the read or write or seek requests. If this bit is set to”0”, the card prohibits these requests.
5	DWF (Drive Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC (Drive Seek Complete)	This bit is set when the drive seeks complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR (CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX (InDex)	This bit is always set to “0”
0	ERR (ERRor)	This bit is set when the previous command has ended is some type of error. The error information is set in the error register. This bist is cleared by the next command.

10. Alternate status register

This register is the same as Status register in physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that –IREQ is not negated when data read.

11. Command register

This register is write only register, and it is used for writing the command to execute the requested operation. The command codes is written in the command register, after the parameter is written is the Task File when the card is in Ready state.

Command	Command code	Used parameter						
		FR	SC	SN	CY	DR	HD	LBA
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1h or 95h	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40h or 41h	N	Y	Y	Y	Y	Y	Y
Recalibrate	1Xh	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6h or 99h	N	N	N	N	Y	N	N
Stand by	E2h or 96h	N	N	N	N	Y	N	N
Stand by immediate	E0h or 94h	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32h or 33h	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

12. Device control register

This register is write only register and it is used for controlling the interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	X	X	X	1	SRST nIEN	nIEN	0

bit	Name	Function
7 to 4	X	Don't care
3	1	This bit is set to "1"
2	SRST(Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0"
1	nIEN(Interrupt Enable)	This bit is used for enabling –IREQ. When this bit is set to "0", -IREQ is enabled. When this bit is set to "1", -IREQ is disabled.
0	0	This bit is set to "0".

13. Drive Address register

The register is read only register, and it is used for confirming the drive status. This register is provides for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	nWTG	nHS3	nHS2	nH1	nHS0	nDS1	nDS0

bit	Name	Function
7	X	This bit remains tri-state when host read access.
6	nWTG (WriTing Gate)	This bit is set as 0
5 to2	nHS3 to Nhs0 (Head Select3-0)	These bits is the negative value of Head Select bits (bit3 to 0) in Drive/Head register.
1	nDS1(Idrive Select1)	This bit is 0 when drive 1 is active and selected.
0	nDS0 (Idrive Select0)	This bit is 0 when drive 0 is active and selected.

5. Physical outline